

WT588D CHIP & MODULE

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1.FEATURES

- *Modules with 16pin, 28pin COB package ,built-in flash memory. Chips with DIP18 or SSOP20 or LQFP32 package. WT588D chip +SPI Flash →WT588D module
- *Duration depends on the SPI flash size, support 2M-32M SPI flash.
- *Built-in high-speed audio processor.
- *Built-in 13Bit D/A convertor, 12Bit PWM output with excellent timbre
- *PWM output can direct drive 0.5W/8Ωspeaker.
- *Support DAC/PWM two kinds of output.
- *support mp3/wav audio files.
- *Vocie can be combined optionally by our PC software, mute can be inserted and will not take up any capacity.
- *Each loaded phrase of voice can be reused in other addresses.
- *Download by USB port, support online and offline download, even the WT588D is power on ,data also can be loaded to SPI flash.
- *Support mp3 control mode, key control mode, 3x8 key combination control mode, parallel control mode , one-line serial control mode, three-line serial control mode, and three-line control I/O extension output mode.
- * Switch to three-line control I/O extension output mode from three-line serial control mode by sending data, working status still keep going in current mode.
- *Set the BUSY signal output mode which show voice playing status optionally.
- * Strong anti-interference, can be used in the industrial field
- *220 controllable addresses, each address can be loaded 128 phrases max, phrases in addresses can be combined to play.
- *Support audition for loaded voice.
- *Enter into sleep mode immediately and waste low power after stop playing
- *15 kinds of key control mode, one button can set one control mode.
- *Equip with WT588D voice chip PC software, make its functions more outstanding.
- *Load 500 phrases voice max for editing
- *Mute duration can be inserted between 10ms to 25minutes
- *17ms reset time
- *Serial baud rate 40us~4000us
- *Working voltage:DC2.8v-5.5v
- *Sleep mode current:10uA
- *10ms key trigger time

*Sampling frequency 6KHz,8KHz,10KHz,12KHz,14KHz,16KHz,18KHz 20KHz

*Support 8 chord MIDI

2. WT588D FUNCTION DESCRIPTIONS

WT588D is a powerful re-programming voice chip microcontroller. Its control mode can be changed and download data to SPI flash by our PC software. This software is easy-operating ,support online download ,even the chip in power on , data can be download to the related SPI flash then reset the circuit, the control mode will be updated.

In the Mp3 control mode, this chip with mp3 player functions , such as play, pause, previous, next, volume up, volume down.

In the key control mode, the trigger mode is flexible, any key can be setted as edge retrigger, edge no retrigger, level unloop, level loop,, level hold loop, prev unloop, next unloop, prev loop, next loop, no function, pause, stop, vol+, vol- and on/off 15 kinds of trigger mode, control 10 key trigger output max.

In the 3x8 key combination control mode,24 addresses' voice can be triggered by edge retrigger mode.

In the parallel control mode, 8 I/O port can be used in controlling max

In the one-line serial control mode, voice play, stop, re-play, volume adjustment can be controlled by MCU.

Three-line serial control mode and three-line serial control I/O port extension mode can be switched , in the three-line control mode, voice play, stop, re-play and volume adjustment can be controlled , or direct trigger voice in 0-219 addresses. In the three-line serial control I/O port extension mode, can extend 8 bit output.

Switch between these two control mode, last working status still keep going in current mode.

PWM output can direct drive 0.5W/8Ω speaker, DAC output connect to external amplifier.

WT588D with a wide range of applications, such as bus reporter, alarm, reminder, alarm clock, study apparatus, household appliances, medical instrument, electronic toys, telecommunication, parking distance control and so on.

3.WT588D SELECTION

MODEL	FLASH	I/O	PACKAGE	KEY MODE	PARALLEL MODE	3X8 MATRIX MODE	MP3 MODE	ONE-LINE SERIAL MODE	THREE-LINE SERIAL MODE
WTW500-16	16M	4	16PIN MODULE	OK	-----	-----	OK	OK	OK
WTW500-28	16M	11	28PIN MODULE	OK	OK	OK	OK	OK	OK
WT588D-18P	EXTERNAL	4	DIP18	OK	-----	-----	OK	OK	OK
WT588D2SS	EXTERNAL	4	SSOP20	OK	-----	-----	OK	OK	OK
WT588D-32L	EXTERNAL	11	LQFP32	OK	OK	OK	OK	OK	OK

4.THE RELATION BETWEEN FLASH CAPACITY AND DURATION

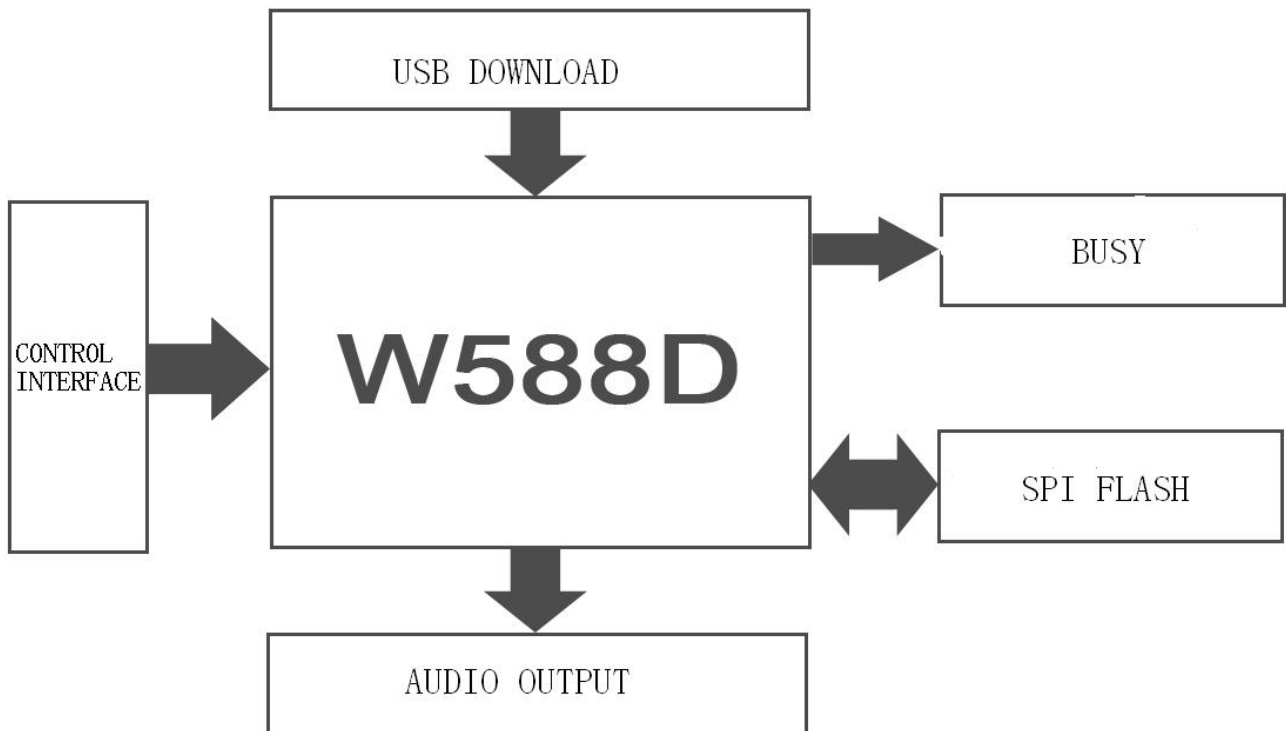
Sampling frequency at 6KHZ

CAPACITY	DURATION	CAPACITY	DURATION	CAPACITY	DURATION
1M	0S	4M	102S	16M	516S
2M	32S	8M	238S	32M	1054S

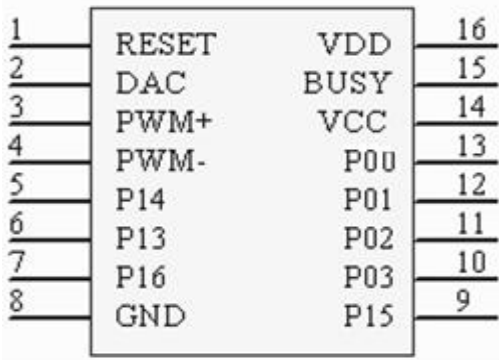
5.APPLICATIONS



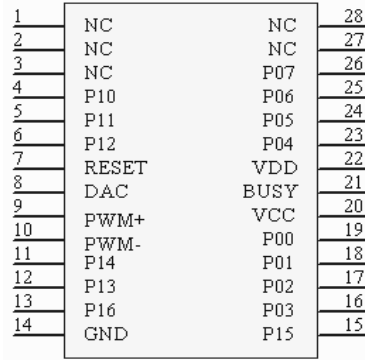
6.WT588D APPLICATION DIAGRAM



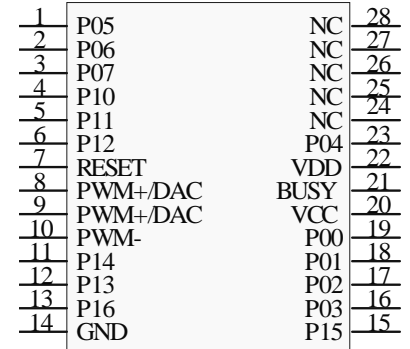
7.PACKAGE SKETCH



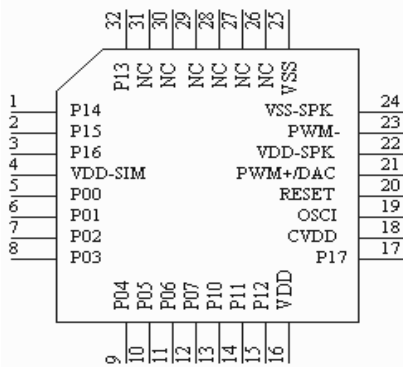
16PIN MODULE



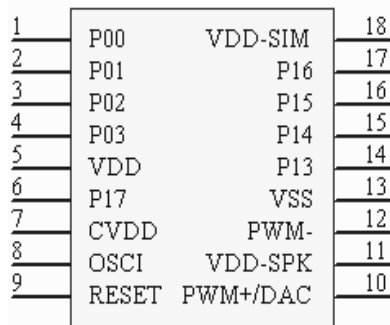
28PIN MODULE (V1.1)



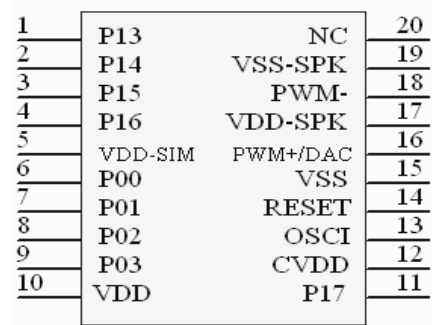
28PIN MODULE (V1.2)



LQPF32 CHIP



DIP18 CHIP



SSOP20 CHIP

8.PIN DESCRIPTIONS

8.1. 16PIN MODULE PIN'S DESCRIPTION

PIN	MARK	BRIET DESCRIPTION	FUNCTION
1	RESET	RESET	RESET PIN
2	PWM+/DAC	PWM+/DAC	PWM+/DAC AUDIO OUTPUT
3	PWM+/DAC	PWM+/DAC	PWM+/DAC AUDIO OUTPUT
4	PWM-	PWM-	PWM- AUDIO OUTPUT
5	P14	DI	PROGRAMMING INPUT
6	P13	DO	PROGRAMMING OUTPUT
7	P16	CLK	CLOCK
8	GND	GND	GROUND
9	P15	CS	PROGRAMMING CHIP-SELECT
10	P03	K4/CLK/DATA	KEY/THREE-LINE CLOCK/ONE-LINE DATA INPUT
11	P02	K3/CS	KEY/THREE-LINE CHIP-SELECT INPUT
12	P01	K2/DATA	KEY/THREE-LINE DATA INPUT
13	P00	K1	KEY INPUT
14	VCC	VCC	MEMORIZER POWER INPUT
15	BUSY	BUSY	PLAY BUSY SIGNAL OUTPUT
16	VDD	VDD	DIGITAL POWER INPUT

8.2. 28PIN MODULE(V1.1) PIN'S DESCRIPTION

PIN	MARK	BRIEF DESCRIPTION	FUNCTION
1	NC	NC	NC
2	NC	NC	NC
3	NC	NC	NC
4	P10	K9/A7/R1	KEY/PARALLEL ADDRESS/MATRIX ROW INPUT/THREE-LINE SERIAL EXTENSION ADDRESS
5	P11	K10/R2	KEY/MATRIX ROW INPUT/THREE-LINE SERIAL EXTENSION ADDRESS
6	P12	R3	MATRIX ROW INPUT/THREE-LINE EXTENSION ADDRESS
7	RESET		RESET
8	PWM+/DAC	PWM+/DAC	PWM+/DAC AUDIO OUTPUT
9	PWM+/DAC	PWM+/DAC	PWM+/DAC AUDIO OUTPUT
10	PWM-	PWM-	PWM- AUDIO OUTPUT
11	P14	DI	PROGRAMMING DATA INPUT
12	P13	DO	PROGRAMMING DATA OUTPUT
13	P16	CLK	PROGRAMMING CLOCK
14	GND	GND	GROUND
15	P15	CS	PROGRAMMING CHIP-SELECT
16	P03	K4/A2/L3/CLK/DATA	KEY/PARALLEL ADDRESS/MATRIX COLUMN/THREE-LINE CLOCK/ONE-LINE DATA INPUT
17	P02	K3/A1/L2/CS	KEY/PARALLEL ADDRESS/MATRIX COLUMN/THREE-LINE CHIP-SELECT INPUT
18	P01	K2/A0/L1/DATA	KEY/PARALLEL ADDRESS/MATRIX COLUMN/THREE-LINE DATA INPUT
19	P00	K1/L0/SBT	KEY/MATRIX COLUMN/SBT PARALLEL ADDRESS TRIGGER OUTPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
20	VCC	VCC	ANALOG POWER INPUT
21	BUSY	BUSY	PLAY BUSY SIGNAL OUTPUT
22	VDD	VDD	DIGITAL POWER INPUT
23	P04	K5/A3/L4	KEY/PARALLEL ADDRESS/MATRIX COLUMN INPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
24	P05	K6/A4/L5	KEY/PARALLEL ADDRESS/MATRIX COLUMN INPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
25	P06	K7/A5/L6	KEY/PARALLEL ADDRESS/MATRIX COLUMN INPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
26	P07	K8/A6/L7	KEY/PARALLEL ADDRESS/MATRIX COLUMN INPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
27	NC	NC	NC
28	NC	NC	NC

8.3. 28PIN MODULE(V1.2) PIN'S DESCRIPTION

PIN	MARK	BRIEF DESCRIPTION	FUNCTION
1	P05	K6/A4/L5	KEY/PARALLEL ADDRESS/MATRIX ROW INPUT/THREE-LINESERIAL EXTENSION ADDRESS
2	P06	K7/A5/L6	KEY/PARALLEL ADDRESS/MATRIX ROW INPUT/THREE-LINE SERIAL EXTENSION ADDRESS
3	P07	K8/A6/L7	KEY/PARALLEL ADDRESS/MATRIX ROW INPUT/THREE-LINE SERIAL EXTENSION ADDRESS
4	P10	K9/A7/R1	KEY/PARALLEL ADDRESS/MATRIX ROW INPUT/THREE-LINE SERIAL EXTENSION ADDRESS
5	P11	K10/R2	KEY/MATRIX ROW INPUT/THREE-LINE SERIAL EXTENSION ADDRESS
6	P12	R3	KEY/MATRIX ROW INPUT/THREE-LINE SERIAL EXTENSION ADDRESS
7	RESET	RESET	RESET
8	PWM+/DAC	PWM+/DAC	PWM+/DAC AUDIO OUTPUT
9	PWM+/DAC	PWM+/DAC	PWM+/DAC AUDIO OUTPUT
10	PWM-	PWM-	PWM- AUDIO OUTPUT
11	P14	DI	PROGRAMMING DATA INPUT
12	P13	DO	PROGRAMMING DATA OUTPUT
13	P16	CLK	PROGRAMMING CLOCK
14	GND	GND	GROUND
15	P15	CS	PROGRAMMING CHIP-SELECT
16	P03	K4/A2/L3/CLK/DATA	KEY/PARALLEL ADDRESS/MATRIX COLUMN/THEREE-LINE CLOCK/ONE-LINE DATA INPUT
17	P02	K3/A1/L2/CS	KEY/PARALLEL ADDRESS/MATRIX COLUMN/THREE-LINE CHIP-SELECT INPUT
18	P01	K2/A0/L1/DATA	KEY/PARALLEL ADDRESS/MATRIX COLUMN/THREE-LINE CHIP-SELECT INPUT
19	P00	K1/L0/SBT	KEY/MATRIX COLUMN/SBT PARALLEL ADDRESS TRIGGER OUTPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
20	VCC	VCC	ANOLOG POWER INPUT
21	BUSY	BUSY	PLAY BUSY SIGNAL OUTPUT
22	VDD	VDD	DIGITAL POWER INPUT
23	P04	K5/A3/L4	KEY/PARALLEL ADDRESS/MATRIX COLUMN INPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
24	NC	NC	NC
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC

8.4. LQFP32 PACKAGE PIN'S DESCRIPTION

PIN	MARK	BRIEF DESCRIPTION	FUNCTION
1	P14	DI	MEMORIZER DATA COMMUNICATIONS INPUT
2	P15	DO	MEMORIZER COMMUNICATIONS CHIP-SELECT
3	P16	CS	MEMORIZER COMMUNICATIONS CLOCK
4	VDD-SI M	CLK	SERIAL POWER INPUT
5	P00	VDD-SIM	KEY/MATRIX COLUMN/SBT PARALLEL ADDRESS TRIGGER OUTPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
6	P01	K2/A0/L1/DATA	KEY/PARALLEL ADDRESS/MATRIX COLUMN/THREE-LINE DATA INPUT
7	P02	K3/A1/L2/CS	KEY/PARALLEL ADDRESS/MATRIX COLUMN/THREE-LINE CHIP-SELECT INPUT
8	P03	K4/A2/L3/CLK/DATA	KEY/PARALLEL ADDRESS/MATRIX COLUMN/THREE-LINE CLOCK/ONE-LINE DATA INPUT
9	P04	K5/A3/L4	KEY/PARALLEL ADDRESS/MATRIX COLUMN INPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
10	P05	K6/A4/L5	KEY/PARALLEL ADDRESS/MATRIX COLUMN INPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
11	P06	K7/A5/L6	KEY/PARALLEL ADDRESS/MATRIX COLUMN INPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
12	P07	K8/A6/L7	KEY/PARALLEL ADDRESS/MATRIX COLUMN INPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
13	P10	K9/A7/R1	KEY/PARALLEL ADDRESS/MATRIX COLUMN INPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
14	P11	K10/R2	KEY/MATRIX ROW INPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
15	P12	R3	MATRIX ROW INPUT/THREE-LINE SERIAL EXTENSION OUTPUT ADDRESS
16	VDD	VDD	CHIP POWER INPUT
17	P17	BUSY	PLAY BUSY SIGNAL OUTPUT
18	CVDD	CVDD	VDD POWER VOLTAGE ADJUSTMENT
19	OSCI	OSCI	CRYSTAL OSCILLATOR INPUT
20	RESET	RESET	RESET
21	PWM+/D AC	PWM+/DAC	PWM+/DAC AUDIO OUTPUT
22	VDD-SP K	VDD-SPK	AUDIO POWER INPUT
23	PWM-	PWM-	PWM- AUDIO OUTPUT
24	VSS-SP K	VSS-SPK	AUDIO POWER GROUND
25	VSS	VSS	GROUND
26	NC	NC	NC
27	NC	NC	NC

28	NC	NC	NC
29	NC	NC	NC
30	NC	NC	NC
31	NC	NC	NC
32	P13	DO	MEMORIZER DATA COMMUNICATIONS OUTPUT

8.5.DIP18 PACKAGE PIN'S DESCRIPTION

PIN	MARK	DESCRIPTION	FUNCTION
1	P00	K1/SBT	KEY/SBT PARALLEL ADDRESS TRIGGER INPUT
2	P01	K2/A0/DATA	KEY/PARALLEL ADDRESS/THREE-LINE DATA INPUT
3	P02	K3/A1/CS	KEY/PARALLEL ADDRESS/THREE-LINE CS INPUT
4	P03	K4/A2/CLK/DATA	KEY/PARALLEL ADDRESS/THREE-LINE CLOCK/ONE-LINE DATA INPUT
5	VDD	VDD	POWER IN
6	P17	BUSY	BUSY OUT
7	CVDD	CVDD	VDD POWER ADJUSTMENT
8	OSCI	OSCI	CRYSTAL OSCILLATOR INPUT
9	RESET	RESET	RESET
10	PWM+/DAC	PWM+/DAC	PWM+/DAC AUDIO OUTPUT
11	VDD-SPK	VDD-SPK	AUDIO POWER INPUT
12	PWM-	PWM-	PWM- AUDIO OUTPUT
13	VSS	VSS	GROUND
14	P13	DO	MEMORIZER COMMUNICATION DATA OUTPUT
15	P14	DI	MEMORIZER COMMUNICATION DATA INPUT
16	P15	CS	MEMORIZER COMMUNICATION CS
17	P16	CLK	MEMORIZER COMMUNICATION CLOCK
18	VDD-SIM	VDD-SIM	SERIAL POWER MANAGEMENT

8.6.SSOP20 PACKAGE PIN'S DESCRIPTION

PIN	MARK	BRIEF DESCRIPTION	FUNCTION
1	P13	DO	MEMORIZER DATA COMMUNICATIONS OUTPUT
2	P14	DI	MEMORIZER DATA COMMUNICATIONS INPUT
3	P15	CS	MEMORIZER COMMUNICATIONS CHIP-SELECT
4	P16	CLK	MEMORIZER COMMUNICATIONS CLOCK
5	VDD-SIM	VDD-SIM	SERIAL POWER MANAGEMENT
6	P00	K1/SBT	KEY/SBT PARALLEL ADDRESS TRIGGER OUTPUT
7	P01	K2/A0/DATA	KEY/PARALLEL ADDRESS/THREE-LINE DATA INPUT
8	P02	K3/A1/CS	KEY/PARALLEL ADDRESS/THREE-LINE CHIP-SELECT INPUT
9	P03	K4/A2/CLK/DATA	KEY/PARALLEL ADDRESS/THREE-LINE CLOCK/ONE-LINE DATA INPUT
10	VDD	VDD	POWER INPUT
11	P17	BUSY	PLAY BUSY SIGNAL OUTPUT
12	CVDD	CVDD	VDD POWER ADJUSTMENT

13	OSCI	OSCI	CRYSTAL OSCILLATOR INPUT
14	RESET	RESET	RESET
15	VSS	VSS	GROUND
16	PWM+/DAC	PWM+/DAC	PWM+/DAC AUDIO OUTPUT
17	VDD-SPK	VDD-SPK	AUDIO POWER INPUT
18	PWM-	PWM-	PWM- AUDIO INPUT
19	VSS-SPK	VSS-SPK	AUDIO POWER GROUND
20	NC	NC	NC

9. PIN'S DETAILED DESCRIPTION

THE USE OF K1 – K10

K1 – K10 defined as I/O port of key trigger ,corresponding I/O port P00 – p07]、 p10 and P11. Switch I/O port level by K1 – k10 or input edge to I/O port, trigger to play the voice. Trigger mode of Key K0 – k9 can be setted as edge retrigger, edge no retrigger, level unloop, level loop, , level hold loop, prev unloop, next unloop, prev loop, next loop, no function, pause, stop, vol+, vol- and on/off 15 kinds of trigger mode.

KEY MODE: P00→K1 P01→K2 P02→K3 P03→K4 P04→K5
 P05→K6 P06→K7 P07→K8 P10→K9 P11→K10

ONE-LINE SERIAL MODE: P00→K1 P04→K5 P07→K8
 P01→K2 P05→K6 P10→K9
 P02→K3 P06→K7 P11→K10

THE USE OF R1-R3、 L0 – L7

In the key control mode of 3x8 matrix, I/O port defined as R – R3、 L0 – L7, R1 – R3 as matrix row input , L0 – L7 as matrix column input. A phrase can be triggered and play when short circuit R and L. In this control mode, all keys trigger mode were defined as EDGE RETRIGGER. The details please find 12.3

The use of SBT and A0-A7

In the parallel control mode, I/O port P00-P07、 P10 defined as SBT, A0-A7. SBT is audition feet, A0-A7 are address, from low to high. I/O port details please find 12.4

10. ELECTRONIC PARAMETERS

($V_{DD} - V_{SS} = 4.5V$, $T_A = 25^{\circ}C$, without load)

PARAMETER	MARK	CONDITION	MIN	TYPICAL	MAX	UNIT
WORKING VOLTAGE	V_{DD}	$F_{sys}=8MHz$	2.8		5.5	v
WORKING CURRENT	I_{OP1}	WITHOUT LOAD	-	4.5	5.5	mA
QUIESCENT CURRENT	I_{DD2}	WITHOUT LOAD	-	1	2	uA
SLEEPING MODE CURRENT	I_{OP2}	WITHOUT LOAD	-	650		uA
LOW VOLTAGE INPUT	V_{IL}	ALL PINS INPUT	V_{SS}	-	$0.3V_{DD}$	V
HIGH VOLTAGE INPUT	V_{IH}	ALL PINS INPUT	$0.7V_{DD}$	-	V_{DD}	V

CURRENT INPUT BP1、BP2、RESET	I _{IN1}	V _{IN} =0V PULL HIGH RESISTANCE=500KΩ	-5	-9	-14	μA
CURRENT INPUT BP1、BP2、RESET	I _{IN2}	V _{IN} =0V PULL HIGH RESISTANCE=150KΩ	-15	-30	-45	μA
CURRENT OUTUT(BPO)	I _{OL}	VDD=3V, VOUT=0.4V	8	12	-	mA
	I _{OH}	VDD=3V, VOUT=2.6V	-4	-6	-	mA
	I _{OL}	VDD=4.5V, VOUT=1.0V	-	25	-	mA
	I _{OH}	VDD=4.5V, VOUT=2.6V	-	-12	-	mA
CURRENT OUTPUT(BP1)	I _{OL}	VDD=3V, VOUT=0.4V	4	10	-	mA
	I _{OH}	VDD=3V, VOUT=2.6V	-4	-6	-	mA
CURRENT OUTPUT PWM+ /PWM-	I _{OL1}	RL=8Ω 【PWM+】 -- 【RL】 --	+200	-	-	mA
	I _{OH1}	【PWM-】	-200	-	-	mA
DAC MAXIMUM CURREN	I _{DAC}	RL=100Ω	-2.4 -4.0	-3.0 -5.0	-3.6 -6.0	mA
PULL HIGH RESISTANCE TEST	R _{PL}		75	150	225	

11.ENVIRONMENTAL LIMITED PARAMETER

PARAMETER	MARK	CONDITION	RATED VALUE	UNIT
POWER	V _{DD} - V _{SS}	-	-0.3~+7.0	V
INPUT VOLTAGE	V _{IN}	ALL INPUT	V _{SS} -0.3~V _{DD} +0.3	V
STORE TEMPERATURE	T _{STG}	-	-55~+150	°C
USING TEMPERATURE	T _{OPR}	-	-40~+85	°C

12.CONTROL MODE

12.1. MP3 MODE

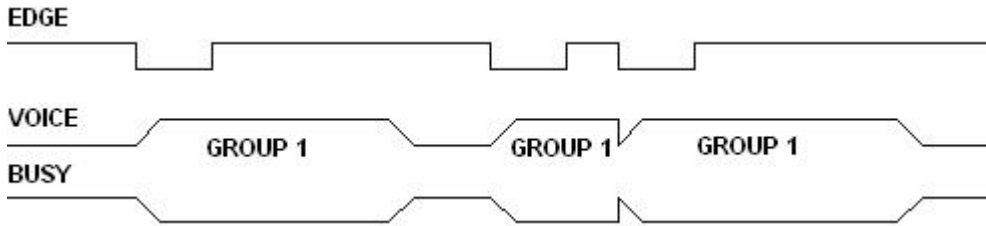
In the mp3 mode, default function of 6 I/O port

I/O	P00	P01	P02	P03	P04	P05
FUNCTION	STOP	PLAY/PAUSE	NEXT	PREVIOUS	VOL+	VOL-

12.2. KEY CONTROL MODE

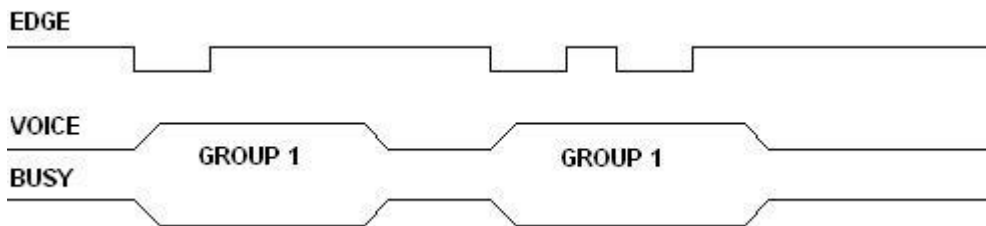
Defined pin can trigger a function of the chip, each pin's trigger mode can be setted solely. Anti-shake time of the key control mode is 10ms. In this mode, include edge retrigger, edge no retrigger, level unloop, level loop, level hold loop, prev unloop, next unloop, prev loop, next loop, no function, pause, stop, vol+, vol- and on/off 15 kinds of trigger mode. Detailed diagram as follows

12.2.1. EDGE RETRIGGER



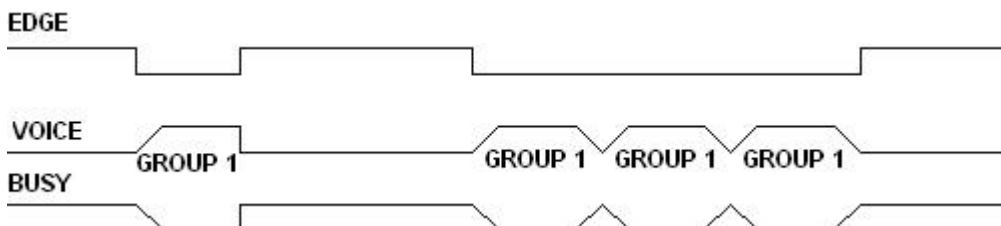
Remark: Negative edge trigger. When the I/O port tested falling edge(such as the I/O short circuit to the ground), the voice can be triggered and play. When in the playing, if another falling edge is tested, the voice will be interrupted and replay.

12.2.2. EDGE NO RETRIGGER



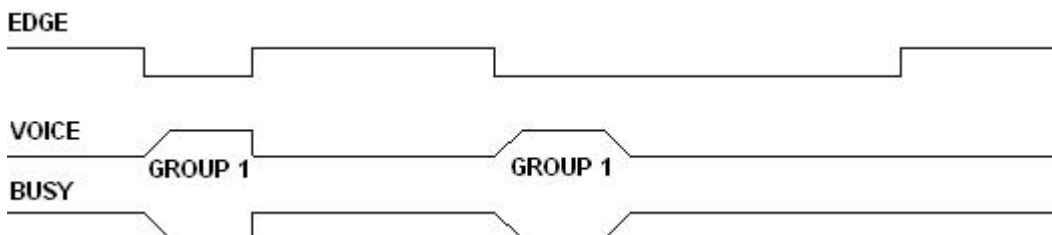
Remark: Negative edge trigger. When the I/O port tested falling edge(such as the I/O short circuit to the ground), the voice can be triggered and play. When in the playing, another falling edge is tested, the voice will not be interrupted.

12.2.3. LEVEL LOOP



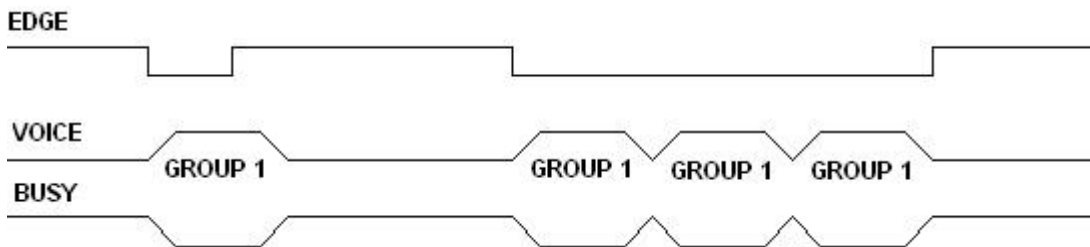
Remark: When the I/O is low level, it will keep playing time and again until turn to high level ,it will stop playing.

12.2.4. LEVEL UNLOOP



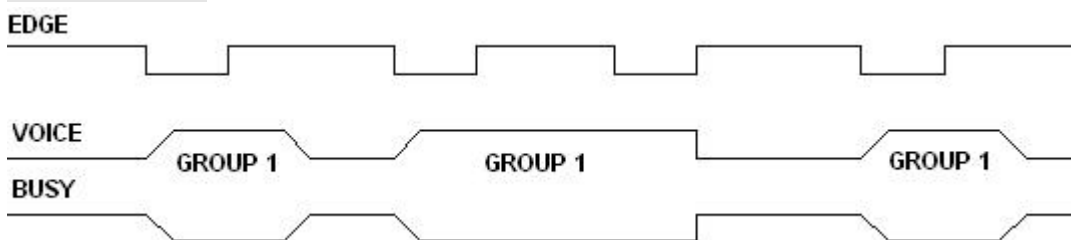
Remark: Level trigger. When the I/O is low level, it will keep playing even turn to high level during the playing until the speech over. If keep low level , it will play time and again.

12.2.5. LEVEL HOLD LOOP



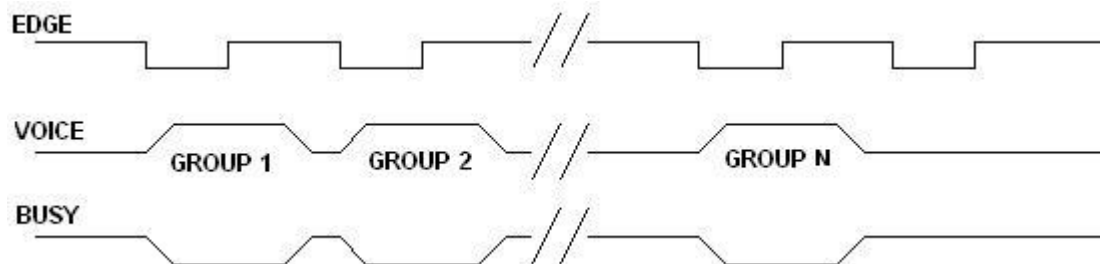
Remark: Negative edge/level trigger. When the I/O is low level, it will keep playing till speech over even turn to high level during the playing. If still keep low level, then it will keep playing time and again.

12.2.6. ON/OFF



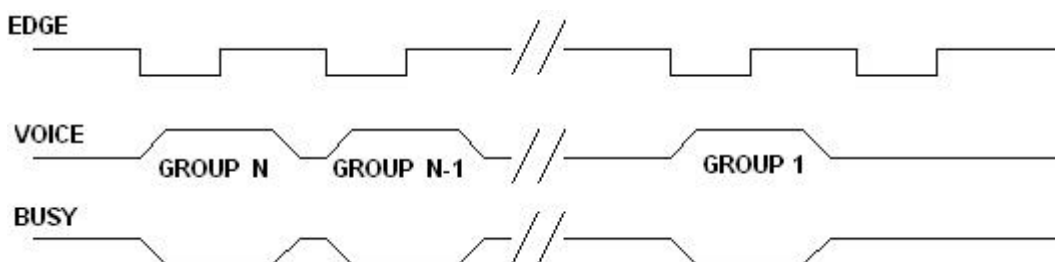
Remark: Negative edge trigger. Negative edge start to play, next negative edge end it.

12.2.7. NEXT UNLOOP



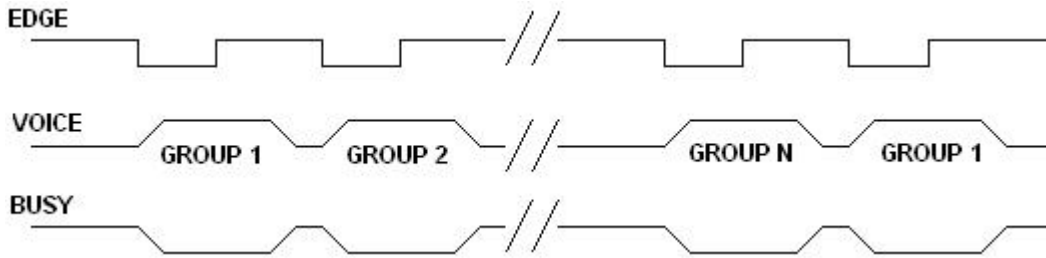
Remark: Negative edge trigger. use one key to trigger. a negative edge trigger a speech, next negative edge trigger next speech till the last speech.

12.2.8. PREV UNLOOP



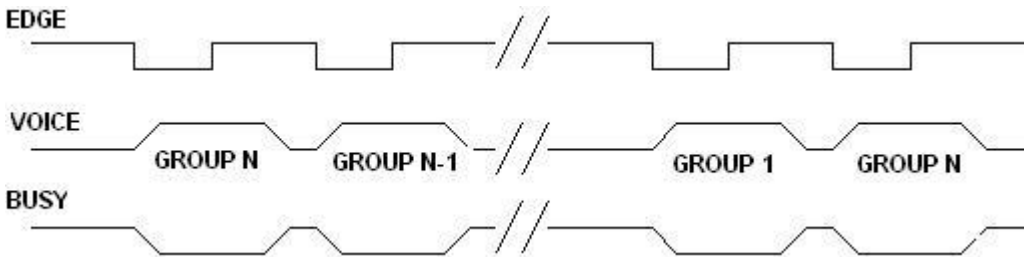
Remark: Negative edge trigger. use one key to trigger. a negative edge trigger a speech, next negative edge trigger previous speech till the last speech.

12.2.9. NEXT LOOP



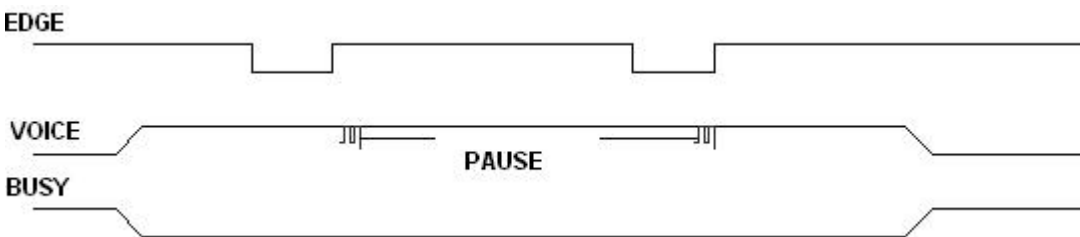
Remark: Negative edge trigger. Use one key to trigger, a negative edge trigger a speech, next edge trigger next speech, circularly.

12.2.10. PREV LOOP



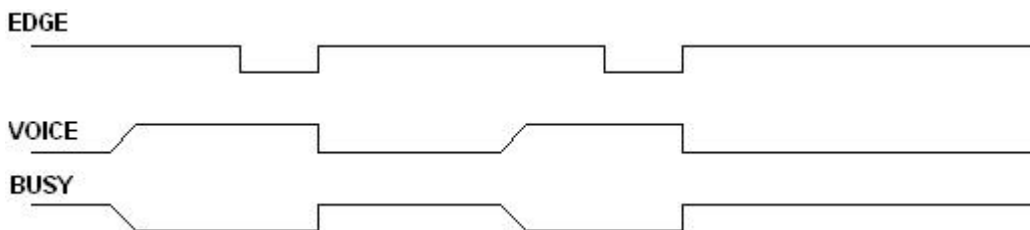
Remark: Negative edge trigger. use one key to trigger. a negative edge trigger a speech, next negative edge trigger previous speech circularly

12.2.11. PAUSE



Remark: Negative edge trigger. First edge make the playing voice to pause, The next edge make it play again. BUSY still keep up during pause.

12.2.12. STOP



Remark: Negative edge trigger. An edge make the playing voice to stop. Next trigger is invalid.

12.3. 3X8 MATRIX KEY CONTROL MODE

In this mode, all keys default as edge retrigger, can trigger 24 speeches, speech addresses can be defined.

I/O	P00	P01	P02	P03	P04	P05	P06	P07
-----	-----	-----	-----	-----	-----	-----	-----	-----

P10	KEY 1	KEY 2	KEY 3	KEY 4	KEY 5	KEY 6	KEY 7	KEY 8
P11	KEY 9	KEY 10	KEY 11	KEY 12	KEY 13	KEY 14	KEY 15	KEY16
P12	KEY 17	KEY 18	KEY 19	KEY 20	KEY 21	KEY 22	KEY 23	KEY24

12.4.PARALLEL CONTRL MODE

In this mode, P00 defined as SBT trigger feet, play speech by changing the address “An”. Pins’ definition as follows

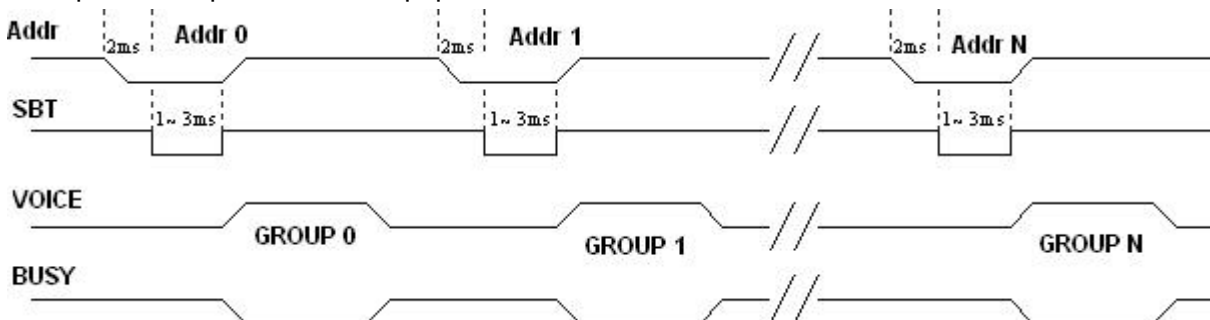
PACKAGE	PIN								
	P00	P01	P02	P03	P04	P05	P06	P07	P10
DIP18	SBT	A0	A1	A2	--	--	--	--	--
SSOP20	SBT	A0	A1	A2	--	--	--	--	--
LQFP32	SBT	A0	A1	A2	A3	A4	A5	A6	A7

12.4.1. SPEECHES AND ADDRESSES CORRESPONDANCE

GROUP N	ADDRESS FEET							
	A7	A6	A5	A4	A3	A2	A1	A0
GROUP0	0	0	0	0	0	0	0	0
GROUP1	0	0	0	0	0	0	0	1
GROUP2	0	0	0	0	0	0	1	0
.....
GROUP217	1	1	0	1	1	0	0	1
GROUP218	1	1	0	1	1	0	1	0
GROUP219	1	1	0	1	1	0	1	1

12.4.2 CONTROL TIMING DIAGRAM

Set the addresses to I/O(P01~P10) by MCU, then play the speech by trigger the SBT feet , the trigger mode can be defined as edge retrigger, edge on retrigger, on/off, prev unloop, next unloop, prev loop, next loop,level unloop, level loop, level hold loop, pause.



During the trigger, address signal maintain 2MS

12.5.ONE-LINE CONTROL MODE

In the serial mode , the user has full control via the serial interface in operating the device.The keys from P00-P10 can configure as any function.

12.5.1. ASSIGNMENT OF I/O

PACKAGE	I/O									
	P00	P01	P02	P03	P04	P05	P06	P07	P10	P11
SOP28	KEY K1	KEY K2	KEY K3	DATA	KEY K5	KEY K6	KEY K7	KEY K8	KEY K9	KEY K10
SSOP28	KEY K1	KEY K2	KEY K3	DATA	KEY K5	KEY K6	KEY K7	KEY K8	KEY K9	KEY K10

12.5.2.COMMAND AND CODE

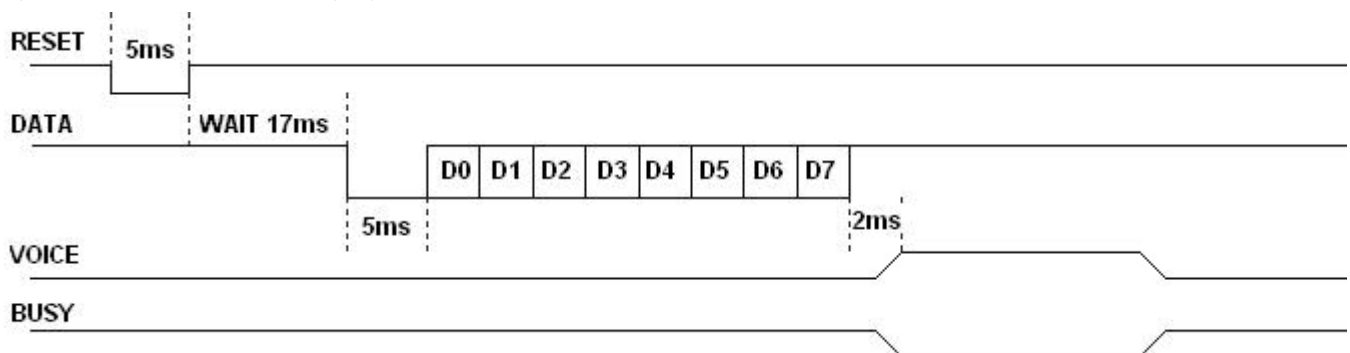
CODE	FUNCTION	DESCRIPTION
E0H	VOLUME ADJUSTMENT	DURING THE PLAYING OR STANDBY, THERE ARE 8 LEVEL VOLUME CAN BE ADJUSTED BY SENDING COMMAND, E0H IS MINIMUM, E7H IS MAXIMUM
F2H	LOOP PLAY	DURING THE PLAY, SPEECH IN CURRENT ADDRESS CAN BE LOOP PALYED BY SENDING COMMAND
FEH	STOP TO PLAY	STOP THE SPEECH

12.5.3.THE RELATIONSHIP BETWEEN SPEECH AND ADDRESS

DATA(HEX)	FUNCTION
00H	PLAY THE SPEECH OF 0
01H	PLAY THE SPEECH OF 1
02H	PLAY THE SPEECH OF 2
.....
D9H	PLAY THE SPEECH OF 217
DAH	PALY THE SPEECH OF 218
DBH	PALY THE SPEECH OF 219

12.5.4.CONTROL TIMING DIAGRAM

One Line Serial mode only need one line,the data bit is depend on the duty cycle. Pull low RESET signal 5ms, wait not less than 17ms in high level, and pull low data signal 5ms before sent out data. The data bit is 0 if duty cycle is 1/3 , and is 1 if duty cycle is 2/3.

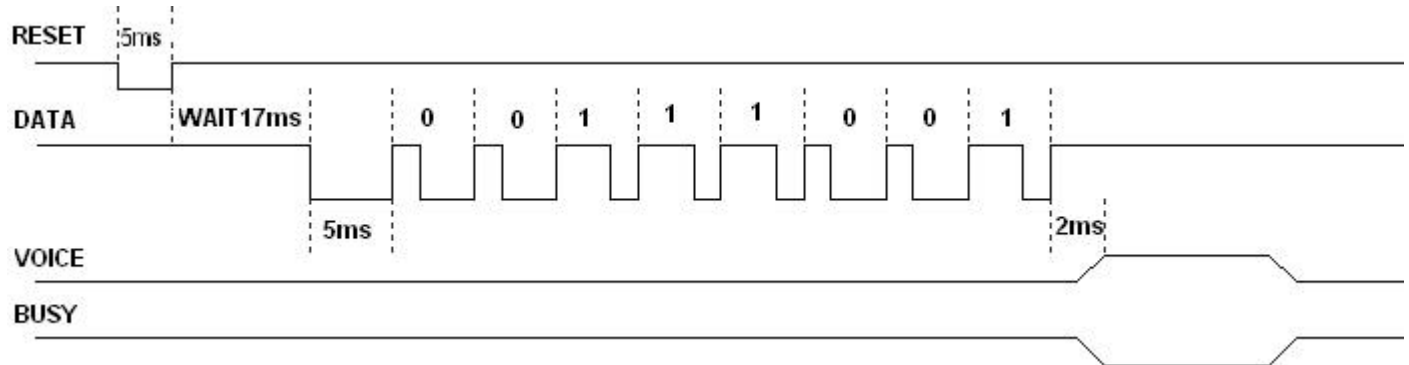


Remark: Reset before sending the data, unless work in interferential environment. DATA is for one-line data communication. Pull low 5ms after reset , for waking up the chip, low level before high level. 2mS after data sent out, BUSY output will be acted.



12.2.5. ONE LINE SERIAL CONTROL DIAGRAM SAMPLE

FOR EXAMPLE, IN THE ONE-LINE CONTROL MODE, THE TIMING OF SENDING DATA 9CH



12.5.5. PROGRAM EXAMPLE

MICROCONTROLLER: PIC16F54, CLOCK SPEED:4MHz

Send oneline(unsigned char addr)

```

{
rst=0; /*reset the chip */
delay1ms(2); /*delay 1ms to 5ms */
rst=1;
delay1ms(6); /*delay 6ms */
sda=0;
delay1ms(5); /* delay 5ms */
for(i=0;i<8;i++)
{ sda=1;
if(addr & 1)
{ delay1us(600); /* 600us */
sda=0;
delay1us(300); } /* 300us */
else {
delay1us(300); /* 300us */
sda=0;
delay1us(600); } /* 600us */
addr>>=1; }
sda=1; }
    
```

12.6.THREE-LINE SERIAL CONTROL MODE

This mode consist of three communication line, they are CS,DATA,SCK, timing imitate the standard SPI means of communication.

12.6.1.ASSIGNMENT OF I/O

PACKAGE	I/O									
	P00	P01	P02	P03	P04	P05	P06	P07	P10	P11
SOP28	--	DATA	CS	SCK	--	--	--	--	--	--

SSOP28	--	DATA	CS	SCK	--	--	--	--	--
--------	----	------	----	-----	----	----	----	----	----

12.6.2. SPEECH AND COMMAND

CODE	FUNCTION	DESCRIPTION
E0H-E7H	VOLUME ADJUSTMENT	DURING THE PLAYING OR STANDBY, THERE ARE 8 LEVEL VOLUME CAN BE ADJUSTED BY SENDING COMMAND, E0H IS MINIMUM, E7H IS MAXIMUM
F2H	LOOP PLAY	DURING THE PLAY, SPEECH IN CURRENT ADDRESS CAN BE LOOP PALYED BY SENDING COMMAND
FEH	STOP TO PALY	THE COMMAND OF STOP PLAYING
F5H	ENTRY I/O EXTENSION OUTPUT	IN THE COMMOND THREE-LINE SERIAL MODE, ENTRY I/O EXTENSION OUTPUT STATE BY SENDING COMMAND
F6H	EXIT I/O EXTENSION OUTPUT	IN THE I/O EXTENSION OUTPUT STATE, ENTRY COMMOND THREE-LINE SERIAL MODE BY SENDING THIS COMMAND

12.6.3. THE RELATIONSHIP BETWEEN SPEECH AND ADDRESS

DATA(HEX)	FUNCTION
00H	PLAY THE SPEECH OF 0
01H	PLAY THE SPEECH OF 1
02H	PLAY THE SPEECH OF 2
.....
D9H	PLAY THE SPEECH OF 217
DAH	PLAY THE SPEECH OF 218
DBH	PLAY THE SPEECH OF 219

12.6.4. THREE-LINE SERIAL CONTROL I/O EXTENSION OUTPUT

In the three-line serial control mode, entry three-line serial I/O extension output by sending data F5H, sending the binary data and make the related I/O to output high level ,sequentially, control the periphery circuit . Send data F6H,will exit this mode, entry commond three-line serial control mode.

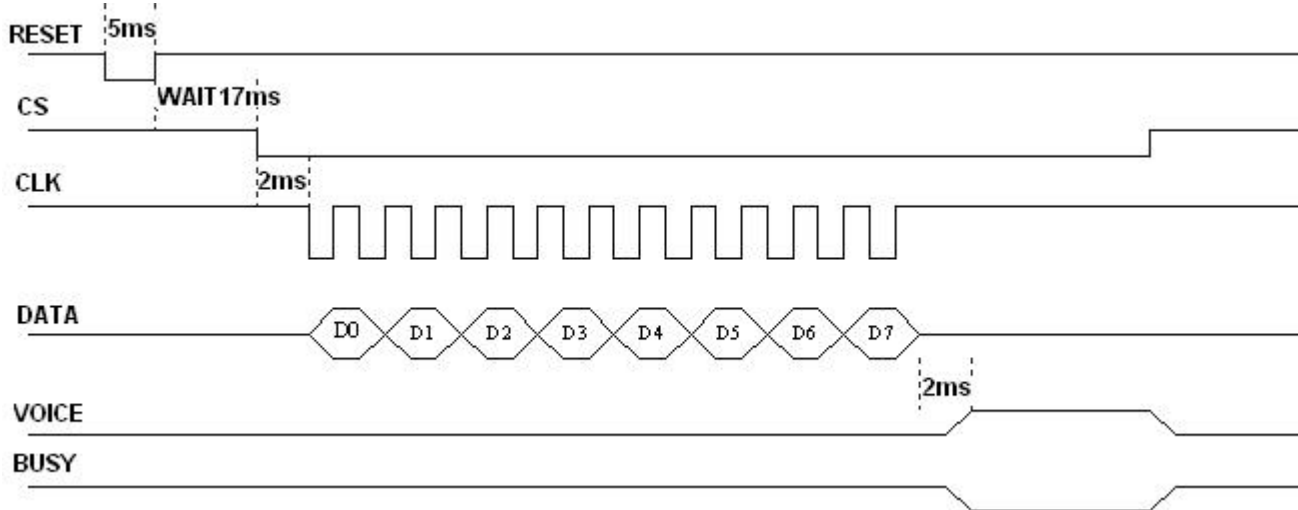
GROUD N	I/O							
	P12	P11	P10	P07	P06	P05	P04	P00
GROUP 0	0	0	0	0	0	0	0	0
GROUP 1	0	0	0	0	0	0	0	1
GROUP 2	0	0	0	0	0	0	1	0
.....
GROUP217	1	1	0	1	1	0	0	1
GROUP218	1	1	0	1	1	0	1	0
GROUP219	1	1	0	1	1	0	1	1

The data in the form, 0 represents low level output, 1 represents high level output. Switch to I/O extension output from three-line serial control mode, the last trigger mode of three-line serial control mode be kept. If setted loop play, the last triggered speech will keep loop playing until switch back to three-line serial mode, and change trigger mode. Switch I/O extension mode to three-line serial control mode, the last I/o extension function also be kept, in the I/O extension output,P00 setted as high level output, after switch to three-line serial control mode, P00 still keep high level output until switch back to I/O extension output and change settings.

I/O extension output can extend 8 I/O, applicate in the situation of poor I/O.

12.6.5. THREE-LINE SERIAL CONTROL TIMING

Three-line serial control mode consist of CS, SCK, DATA, timing imitate standard SPI communication mode, pull low 1ms-5ms before reset signal send out code. During working, RESET pin should keep high when chip is working. CS should keep low 2ms-10ms to wake up the chip, data LSB first, data clock in chip in rising edge. clock cycle is 40us-2ms. BUSY signal will active in 2ms after data transmit success. Low first, then high, when transmit data. Timing diagram as follow:



12.6.6. PROGRAM EXSAMPLE

(Microcotroller PIC16F54, system speed 4MHz)

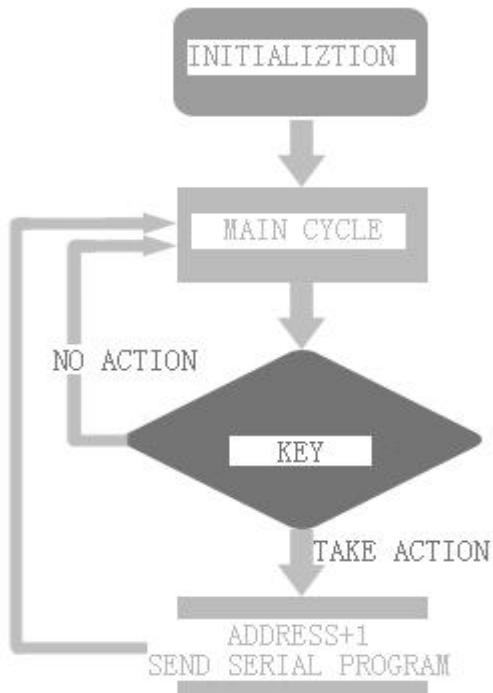
Send threelines(unsigned char addr)

```

{rst=0;
delay1ms(5);rst=1;
delay1ms(17);
cs=0;
delay1ms(2);
for(i=0;i<8;i++)
{ scl=0;
if(addr & 1)sda=1;
else sda=0;
addr>>=1;
delay1us(30);
scl=1;
delay1us(30);    }
cs=1;}
    
```

13. CONTROL TIMING

13.1.CONTROL TIMING DIAGRAM



13.2. ONE-LINE SERIAL CONTROL PROGRAMMING

This program only for one-line serial control mode application circuit in “WT588D CHIP&MODULE DETAILED INFORMATION”.

```

    ORG 0000H
    KEY EQU P1.1    ;key pin
    RST EQU P1.4    ;reset pin
    SDA EQU P3.0    ;data pin
    DAIFAZHI EQU 50H    ;send code value temp
    MOV DAIFAZHI,#0H;intial send value 0
    MOV R5,#8        ;loop eight times
    
```

MAIN:

```

    JB KEY,MAIN
    MOV R6,#20      ;delay 20MS
    LCALL DELAY1MS
    JB KEY,MAIN    ;key press debounce
    JNB KEY,$      ;wait key pressed release
    LCALL one_line ;call one line program
    INC DAIFAZHI   ;send value add 1
    MOV A,DAIFAZHI
    CJNE A,#210,XX2 ;
    XX2: JC XX3
    MOV DAIFAZHI,#0H
    XX3: LJMP MAIN
    
```

```

one_line:          ;///one line send code subprogram
    CLR RST
    MOV R6,#5      ;delay5MS
    LCALL DELAY1MS
    SETB RST
    MOV R6,#17     ;delay17MS
    LCALL DELAY1MS
    CLR SDA
    MOV R6,#5      ;delay5MS
    LCALL DELAY1MS
    MOV A,DAIFAZHI
LOOP:   SETB SDA
    RRC A
    JNC DIDIANPIN ;high level  high:low=2:1
    LCALL DELAY200US
    LCALL DELAY200US
    CLR SDA
    LCALL DELAY200US
    LJMP LOOP1
DIDIANPIN:         ;low level  low:high=1:2
    LCALL DELAY200US
    CLR SDA
    LCALL DELAY200US
    LCALL DELAY200US
LOOP1:  DJNZ R5,LOOP
    MOV R5,#08H
    SETB SDA
    RET
DELAY200US: MOV R6,#100          ;delay 400US subprogram
    DJNZ R6,$
    RET
DELAY1MS:         ;delay 1mssub program, change r6 value can change delay time
L1:  MOV R7,#248
    DJNZ R7,$
    DJNZ R6,L1
    RET
    END

```

13.3. ONE-LINE SERIAL CONTROL “C” PROGRAMMING LANGUAGE

This program only for one-line serial control mode application circuit in “WT588D CHIP&MODULE DETAILED INFORMATION”.

```

#include <at89x2051.H>
sbit KEY=P1^1; /*P1_1 is P1 bit2*/

```

```
sbit RST=P1^4^; /*P1_4 is bit3*/
sbit SDA=P3^0; /*P3_0 is bit4*/
void delay1ms(unsigned char count) //1MS delay subprogram
{
unsigned char i,j,k;
for(k=count;k>0;k--)
    for(i=2;i>0;i--)
        for(j=248;j>0;j--);
}

void delay100us(unsigned char count) //100US delay subprogram
{ unsigned char i;
unsigned char j;
    for(i=count;i>0;i--)
        for(j=50;j>0;j--);
}

Send_online(unsigned char addr)
{
unsigned char i;
RST=0;
delay1ms(5);          /*wait reset delay 5MS*/
RST=1;
delay1ms(17);        /* delay 17ms */
SDA=0;
delay1ms(5);         /* delay 5ms */
for(i=0;i<8;i++)
    {SDA=1;
    if(addr & 1)
        {delay100us(4);    /* 400us */
        SDA=0;
        delay100us(2);    /* 200us */
        }
    else {
        delay100us(2);    /* 200us */
        SDA=0;
        delay100us(4);    /* 400us */
        }
    addr>>=1; }
    SDA=1;
}

main()
{unsigned char FD=0;
P3=0XFF;
while(1)
```

```

{
if(KEY==0)
{
delay1ms(10);
if(KEY==0) //press key P1.1 increase by decrease key value
{
Send_online(FD);
FD++;
if(FD==210) //one line control mode, control 210 sectors at best
{
FD=0;
}
while(KEY==0); //wait key pressed release, debounce time
}
}
}
}

```

13.4. THREE-LINE SERIAL CONTROL PROGRAMMING

This program only for three-line serial control mode application circuit in “WT588D CHIP&MODULE DETAILED INFORMATION”.

ORG 0000H

```

KEY EQU P1.1 ;key pin
RST EQU P1.4 ;reset pin
CS EQU P3.1 ;CS trigger pin
SCL EQU P3.2 ;clock pin
SDA EQU P3.0 ;data pin
DAIFAZHI EQU 50H ;send value temp address
MOV DAIFAZHI,#0H;intinal send value 0
MOV R5,#8 ;loop eight times

```

MAIN:

```

JB KEY,MAIN
MOV R6,#20 ;delay 20MS
LCALL DELAY1MS
JB KEY,MAIN ;key debounce
JNB KEY,$ ;wait key pressed release
LCALL THREE_LINE;call three line subprogram
INC DAIFAZHI ;send value add 1
MOV A,DAIFAZHI
CJNE A,#220,XX2 ;judge the sector address if at max
XX2: JC XX3
MOV DAIFAZHI,#0H
XX3: LJMP MAIN

```

THREE_LINE: ;///three line subprogram

```

        CLR RST
        MOV R6,#5      ;delay 5MS
        LCALL DELAY1MS
        SETB RST
        MOV R6,#17    ;delay 17MS
        LCALL DELAY1MS
        CLR CS
        MOV R6,#2     ;delay 2MS
        LCALL DELAY1MS
        MOV A,DAIFAZHI
LOOP:
        CLR SCL
        RRC A
        MOV SDA,C
        LCALL DELAY50US
        SETB SCL
        LCALL DELAY50US
        DJNZ R5,LOOP
        MOV R5,#08H
        SETB CS
        RET
DELAY50US:  MOV R6,#25      ;delay 50US subprogram
            DJNZ R6,$
            RET
DELAY1MS:   ;delay 1ms,change r6 value can change delay time
L1:        MOV R7,#248
            DJNZ R7,$
            DJNZ R6,L1
            RET
            END

```

13.5. THREE-LINE SERIAL CONTROL “C” PROGRAMMING LANGUAGE

This program only for three-line serial control mode application circuit in “WT588D CHIP&MODULE DETAILED INFORMATION”.

```

#include <at89x51.H>
sbit KEY=P1^1; /*P1_1 P1 bit2*/
sbit RST=P1^4; /*P1_4 P1 bit3*/
sbit CS=P3^1; /*P3_1 P1 bit4 */
sbit SCL=P3^2; /*P3_2 P3 bit3*/
sbit SDA=P3^0; /*P3_0 P3 bi1*/
//sbit DENG=P3^7; /*P3_5 P3 bit6*/
void delay1ms(unsigned char count) //1MS delay subprogram
{
unsigned char i,j,k;
for(k=count;k>0;k--)
    for(i=2;i>0;i--)
        for(j=248;j>0;j--);
}

```

```
}

void delay100us(void) //100US delay subprogram
{
unsigned char j;
    for(j=50;j>0;j--);
}

Send_threelines(unsigned char addr) //three line send code subprogram
{unsigned char i;
    RST=0;
    delay1ms(5);
    RST=1;
    delay1ms(17);        /* 17ms*/
    CS=0;
    delay1ms(2);
for(i=0;i<8;i++)
    {SCL=0;
    if(addr & 1)SDA=1;
    else SDA=0;
    addr>>=1;
    delay100us(); /* 100us */
    SCL=1;
    delay100us();
    }
    CS=1;
}

main()
{unsigned char FD=0;
    P3=0XFF;
    while(1)
    {
    if(KEY==0)
    {
        delay1ms(20);
        if(KEY==0) // press key P1.1 increase by decrease key value
        {
            Send_threelines(FD);
            FD++;
            if(FD==220// three line control mode, control 220 sectors at best
                FD=0;
            }
            while(KEY==0); //wait key pressed release
        }
    }
}
```

```
}  
}
```

14.VERSION

VERSION	DATE	DESCRIPTION
V1.4	2008-9-12	ORIGINAL